

## Audio Noise in Systems mixing older 8-port Cards with TRIBUS / MADI / AIO-16s

Issue Severity:	Product(s) Affected:
<input type="checkbox"/> <b>High:</b> URGENT – Immediate Action Required  <input checked="" type="checkbox"/> <b>Medium:</b> Bosch Security Systems, Inc. strongly recommends you take the action(s) described below.  <input type="checkbox"/> <b>Low:</b> Advisory	<ul style="list-style-type: none"> <li>ADAM Systems using TRIBUS / MADI / AIO-16 as clock master when 8-port style cards (AIO-8 / RVON-8 / AES-3 / DBX) also deployed in frame</li> </ul>
Notification Applies To:	Access Restrictions:
<input checked="" type="checkbox"/> Technical Support (TSS) <input checked="" type="checkbox"/> Repair (ASA) <input checked="" type="checkbox"/> Sales (NSO / RSO)	<input type="checkbox"/> Internal Distribution <b>ONLY</b> <input checked="" type="checkbox"/> <b>No</b> Restrictions (Internal & External Distribution)

### 1.0 Issue

Engineering has become aware of several systems deployed at customer sites in which newer cards used as a clock master (specifically TRIBUS / MADI / AIO-16) have generated noise with older generation cards (AIO-8 / AES-3 / RVON-8 / DBX). This combination has produced audio noise on timeslots associated with the older generation cards.

The symptoms of this problem are as follows:

- Applicable to ADAM frames only (ADAM-M not formally approved for use of AIO-8, RVON-8, AES-3, DBX)
- TRIBUS, MADI or AIO-16 is clock master for frame
- Typically, both clock master cards are TRIBUS, MADI or AIO-16
- Frame also populated with AIO-8, RVON-8, AES-3 or DBX cards
- Audible noise generated on TDM timeslots connected assigned to older generation cards

If this issue is suspected, it can typically be proven by removing one of the two clock master cards to see if the noise is reduced or goes away. In many systems, this action of removing one of the two clock master cards is sufficient to eliminate the noise.

The root cause of this problem is that the clock generation circuits on the various ADAM cards have not been consistently designed over time. Any I/O card in the ADAM architecture is capable of serving as the clock master for a system and possesses the ability to generate the reference clocks for all the other cards in the frame. In addition to the ability for each card to generate reference clocks for the other cards, it also can receive a clock reference from any other card serving as clock master.

The older system cards (AIO-8 / RVON-8 / AES-3 / DBX) all need to see an incoming clock reference that complies with 5 V CMOS thresholds (typically a logic high level of 3.6 Vdc or greater). The TRIBUS, MAD1 and AIO-16 cards all generate clock outputs which are TTL levels. These measure approximately 3 V in the lab but can be as low as 2.15 V depending upon signal integrity. The fact that these 3 newer cards do not drive clock reference levels appropriate for the older generation cards causes instability in the clocks received by the AIO-8 / RVON-8 / AES-3 / DBX cards. The instability creates jitter and sampling errors on the TDM bus. This introduces audible noise in the system.

**Table 1: Clock Drive / Receive Technology Levels for ADAM Cards**

CARD		Driver PN	Clock Ref Output Level?			Receiver PN	Clock Ref Input Level?
AIO-8	U23	49FCT805ASOG	5 V CMOS		U5	CY7B992-5JC	5 V CMOS
RVON-8	U90	49FCT805ASOG	5 V CMOS		U80	CY7B992-5JC	5 V CMOS
AES-3	U32	49FCT805ASOG	5 V CMOS		U20	CY7B992-5JC	5 V CMOS
AIO-16	UH01	49FCT805CTQG	3 V TTL		UD01	CY7B991V-2JC	3 V TTL
RVON-16	U49	49FCT805ASOG	5 V CMOS		U48	CY7B991V-2JC	3 V TTL
MADI-16	UC02	49FCT805CTQG	3 V TTL		UC04	CY7B991V-2JC	3 V TTL
OMI	U5	49FCT805ASOG	5 V CMOS		U4	CY7B991V-2JC	3 V TTL
Tribus TBX	UC02	49FCT805CTQG	3 V TTL		UC04	CY7B991V-2JC	3 V TTL
Dual Bux DBX	U32	49FCT805ASOG	5 V CMOS		U5	CY7B992-5JC	5 V CMOS

Note that two of the newer generation cards (RVON-16 and OMI OMNEO card) do drive the appropriate clock reference levels even for the older cards. The only issues will occur when the TRIBUS / MADI / AIO-16 are used as clock masters for the older cards.

## 2.0 Resolution / Corrective Actions

In order to fix this problem, the clock drivers on the TRIBUS, MADI and AIO-16 must be replaced with a footprint compatible device capable of driving a 5 V compliant output. The TRIBUS and MADI cards currently use the same Front Card PCB layout, so both of these cards can be fixed by replacing UC02. For the AIO-16, UH01 needs to be replaced.

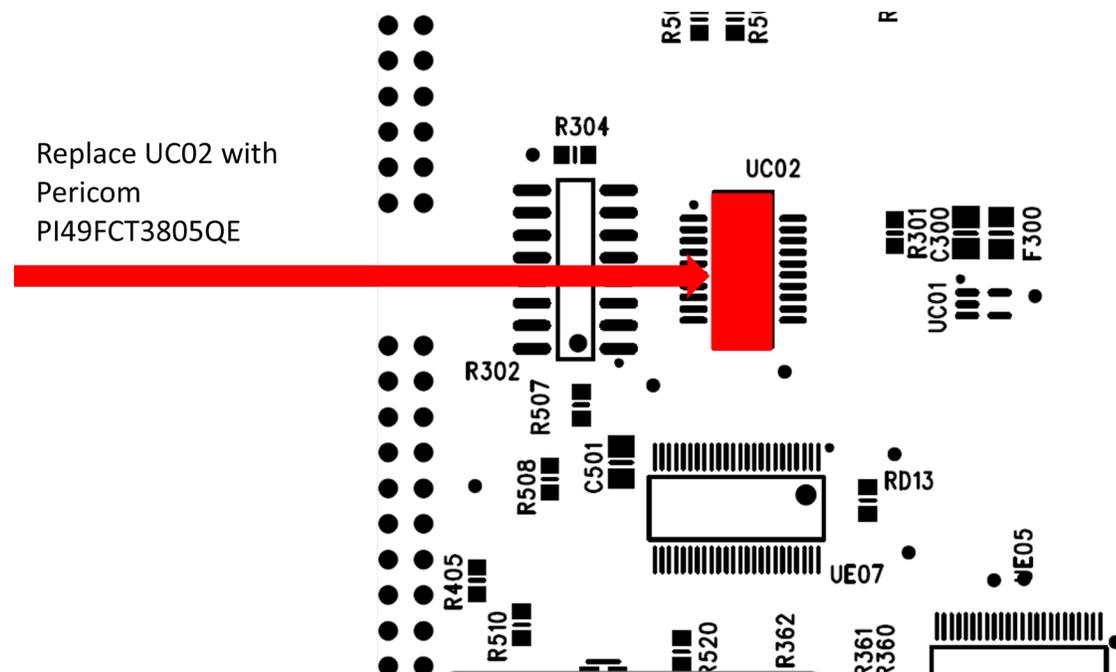
In the case of the TRIBUS and MADI designs, replacement of the clock driver device with a 5 V compliant output actually creates another issue which must be resolved. Every I/O card that is clock master also generates a reference clock onto the backplane which comes back into that card on backplane connector pin A20 as its own clock reference. In the case of the TRIBUS and MADI, this incoming clock reference goes through a 33 Ohm series resistor into an FPGA. The FPGA is designed for 3.3 V compliant inputs, but will tolerate levels up to 4.1 V maximum. The change to a 5 V output level will potentially damage these parts.

In order to mitigate this risk of damage, an additional diode clamp must be reworked onto the PCBA to limit the incoming clock reference level to the FPGA. This diode clamps the reference clock input to a level approximately a diode drop above 3.3 Vdc. This same risk is not present on the AIO-16 and does not need to be implemented.

Engineering changes are in process to incorporate these changes on all AIO-16, Tribus and MADI cards produced after November 2013.

## 3.0 TRIBUS / MADI Clock Generator IC Rework

STEP 1: Remove UC02. Clean pads and install Pericom PI49FCT3805QE device.

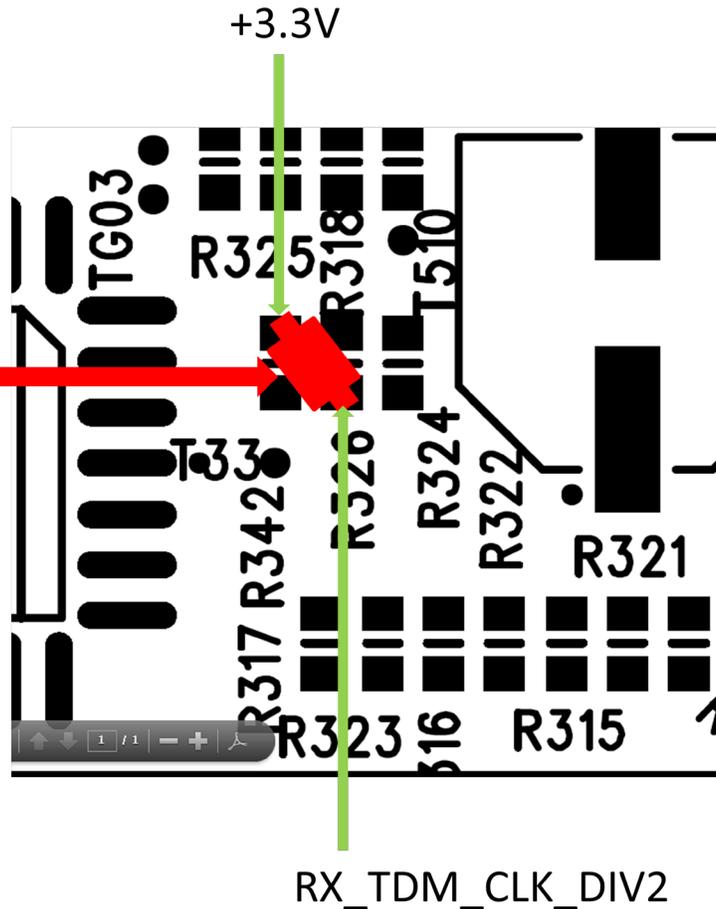


STEP 2: Solder diode across following parts to clamp incoming clock reference signal to +3.3 Vdc rail:

Infineon  
BAT1503WE6327  
Schottky  
Clamp  
Diode  
SOD-323

Carefully place  
diode across R326  
and R342. Solder into  
position.

Cathode connects to  
+3.3V, anode connects  
to RX\_TDM\_CLK\_DIV2



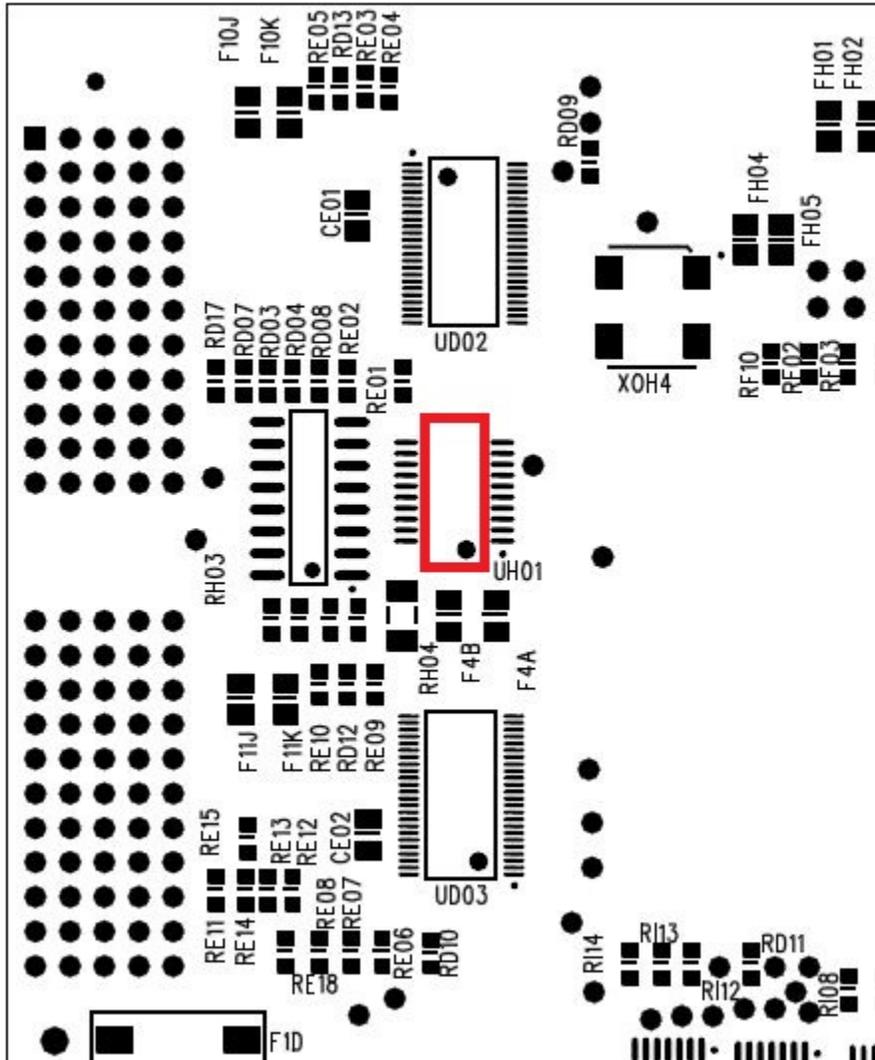
STEP 3: Reworked board should be re-tested to verify issues have been corrected and unit is still functioning correctly in all other areas.

# RTS™ TECHNICAL BULLETIN

## 4.0 AIO-16 Clock Generator IC Rework

STEP 1: Remove UH01.

STEP 2: Clean pads and install Pericom PI49FCT3805QE device at location shown in photo below.



STEP 3: Reworked board should be re-tested to verify issues have been corrected and unit is still functioning correctly in all other areas.

**NOTICE!**

This bulletin should also be read in conjunction with RTS-TB-021 and RTS-TB-023 which also address audible noise problems in the ADAM / ADAM-M frames.

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**NOTICE!**

As stated in this bulletin, the potential exists that an unmodified TRIBUS or MADI card could have the FPGA damaged by a 5 V level clock reference input (this was the reason for the diode clamping rework). The Tribus cards are usually allocated as clock masters in the system and would likely not be susceptible to any issues outside of those described in this bulletin. The potential does exist today that an unmodified MADI card could be operated in a chassis where the clock master is any of the cards in Table 1 which can drive a 5 V output level (example: RVON-16 or OMI module). This would typically be a configuration produced by a field upgrade mixing old and new equipment and is not likely for systems shipping directly from the factory.

In this case, the FPGA clock reference input (3.3 V tolerant) on the MADI card could be subject to damage over time by the 5 V clock levels on the backplane reference. This damage has not been observed in any deployed systems, but it is a technology risk. Technical support should be aware of this potential issue when reviewing customer configurations in conjunction with this problem.

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